UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,930	01/13/2005	Tommi Koistinen	60282.00238	7618

32294 7590 11/20/2007

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
TAHA, SHAQ	

ART UNIT	PAPER NUMBER
2146	

MAIL DATE	DELIVERY MODE
11/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,930	KOISTINEN ET AL.	
	Examiner	Art Unit	
	Shaq Taha	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26 - 53* is/are pending in the application.

4a) Of the above claim(s) *38 - 40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26 - 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 26 - 53 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26 - 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al (US 6,272,522).

- Regarding claim 26, Lin teaches a method for balancing the load of resources in a packet switched connection, **[A data packet switching and server load balancing device is provided, (See Abstract) & Fig. Wherein the it discloses the load balancing between the switching processors];**

within a communication system **[respective external networks for receiving and sending data packets via a particular communication protocol, (See Abstract)]**;

said system comprising processing units for performing communication, **[computer system comprises a plurality of symmetrical processors coupled together by a common data bus, (See Abstract)]**, at least one load balancing unit for distributing the load to said processing units, **[The control processor receives raw load status data from the external networks and generates load distribution configuration data therefrom, (See Abstract)]**;

and a data storage, **[Fig. 4, Ref # 34]**;

said method comprising: obtaining a current connection state as well as a current load state of said processing units from said data storage, **[The switching processor obtains the current load distribution data from the active buffer, (Column 7, lines 12 – 13) & (Fig. 13, Ref # 342)]**;

selecting by said load balancing unit a processing unit on a per packet basis irrespective of a specific connection to which a respective packet belongs, **[In addition, the switching processors re-write the routing information included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract) & Fig. 3, Ref # 20 wherein a unit per packet is disclosed]**;

maintaining information about the load state of each processing unit, **[A routing daemon within the control processor is a program that executes in the**

background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)];

so that said selecting step is performed by selecting a processing unit to serve and process a respective packet based on the load state, **[The switching processors route received ones of the data packets to a selected one of the external networks in accordance with information included in a header portion of the data packets and the load distribution configuration data, (See Abstract)].**

- Regarding claim 27, Lin teaches a method wherein said data storage is accessed by said load balancing unit, **[The load distribution configuration data is stored in the main memory for access by the data packet switching processors, (See Abstract)].**

- Regarding claim 28, Lin teaches a method wherein said data storage is accessed by said processing units, **[The load distribution configuration data is stored in the main memory for access by the data packet switching processors, (See Abstract)].**

- Regarding claim 29, Lin teaches a method wherein said information about the load state is maintained as a Boolean state, **[it is inherent to use a Boolean**

value, since it is a digital or analog that depends on 1s and 0s, or true and false].

- Regarding claim 30, Lin teaches a method wherein a processing unit is selected in a round-robin fashion, **[it is inherent to use a round-robin fashion, since it is describes correspondence authored or signed by numerous individuals to a single address].**

- Regarding claim 31, Lin teaches a method wherein a supported service profile for each processing unit is maintained, **[The connection table maintains a record of the TCP and UDP connections routed by each of the switching processors, (Column 7, lines 25 – 27)].**

- Regarding claim 32, Lin teaches a method wherein said supported service profile is used as additional selection criteria. **[At any given time, one of the two memory buffers is the active buffer and the other is the back-up buffer, (Column 7, lines 8 – 10)].**

- Regarding claim 33, Lin teaches a method wherein said load balancing unit is configured to obtain a load state from each processing unit upon a hardware based mechanism, **[As illustrated in FIG. 8, the control processor does not have a direct connection to the network drivers. Instead, the pseudo-**

network driver is configured to appear to the user application programs as a hardware network interface, (Column 11, lines 10 – 14)].

- Regarding claim 34, Lin teaches a method wherein said load balancing unit is configured to obtain a load state from each processing unit upon a packet based mechanism, **[It is anticipated that the load balancing and packet switching device remain continuously in an operational state, and so this initialization step may only be executed rarely, (Column 8, lines 19 – 22)].**

- Regarding claim 35, Lin teaches a method wherein a load state of a processing unit is inserted into a packet processed by said unit, **[The switching processors route received ones of the data packets to a selected one of the external networks in accordance with information included in a header portion of the data packets and the load distribution configuration data, (See Abstract)].**

- Regarding claim 36, Lin teaches a method wherein a packet returned by a processing unit is interpreted as a flag for a free resource, **[After step 106, the packet engine module 72 returns to step 102. This first processing loop will repeat indefinitely until a received data packet is detected at step 104, (Column 8, lines 34 – 37)].**

- Regarding claim 37, Lin teaches a method wherein excess traffic is redirected to another load balancing unit, said excess traffic being defined upon the number of active processing units, **[Routers read the network address in each transmitted data packet and make a decision on how to send it based on the most expedient route (traffic load, line costs, speed, bad lines, etc.), (Column 4, lines 43 – 46)].**

- Regarding claim 38, Lin teaches a device unit for serving and processing packets of a communication connection, **[A data packet switching and server load balancing device is provided by a general-purpose multiprocessor computer system, (See Abstract)];**

  comprising: means adapted to inform a load state of said device to a balancing unit, **[FIG. 4 is a block diagram depicting communication of information between the control processor and one of the switching processors, (Column 3, lines 35 – 37)];**

  and means adapted to obtain a state of said communication connection, **[It is anticipated that the load balancing and packet switching device remain continuously in an operational state, and so this initialization step may only be executed rarely, (Column 8, lines 19 – 22)].**

  wherein said device unit is adapted to serve and process packets of plural connections, **[A first one of the processors is adapted to serve as a control**

processor and remaining ones of the processors are adapted to serve as data packet switching processors, (See Abstract)].

- Regarding claim 39, Lin teaches a device unit wherein said obtaining means is adapted to retrieve said communication connection state from a data storage, **[If the packet switching processor determines at step that the intended destination for the data packet is one of the user applications running on the control processor, the data packet is written into the data packet storage location of the shared memory, (Column 39 – 43)].**

- Regarding claim 40, Lin teaches a device unit wherein said obtaining means is adapted to retrieve said communication connection state from a packet being under processing, **[If the packet switching processor determines at step that the intended destination for the data packet is one of the user applications running on the control processor, the data packet is written into the data packet storage location of the shared memory, (Column 39 – 43)].**

- Regarding claim 41, Lin teaches a device unit for balancing a load of each of multiple processing units performing a packet switched communication connection, **[A data packet switching and server load balancing device is provided by a general-purpose multiprocessor computer system, (See Abstract)];**

comprising: means for maintaining a load state of each of said processing units, **[A routing daemon within the control processor is a program that executes in the background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)];**

and means adapted to select a processing unit on the basis of a respective load state on a per packet basis irrespective of a specific connection to which a respective packet belongs, **[In addition, the switching processors re-write the routing information included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract)];**

- Regarding claim 42, Lin teaches a device wherein a load state of a processing unit is contained in a table, **[The shared memory further includes a routing table, a configuration table, and a connection table, (Column 6, lines 55 – 56)].**

- Regarding claim 43 Lin teaches a device wherein a load state of a processing unit is expressed as a Boolean value, **[it is inherent to use a Boolean value, since it is a digital or analog that depends on 1s and 0s, or true and false].**

- Regarding claim 44, Lin teaches a device wherein a load state of a processing unit is expressed as value which corresponds to the percentage of load, **[This**

raw data includes various factors, including the number of clients presently being served, the utilization rates of the CPU and memory of the application server processor, the average execution time, and the number of requests per second, (Column 6, lines 39 – 43)].

- Regarding claim 45, Lin teaches a device wherein said selecting means is adapted such that a processing unit is selected also on the basis of a parameter indicating the service profile supported by a respective processing unit, **[This raw data includes various factors, including the number of clients presently being served, the utilization rates of the CPU and memory of the application server processor, the average execution time, and the number of requests per second, (Column 6, lines 39 – 43) & (Fig. 2)].**

- Regarding claim 46, Lin teaches a device wherein said parameter is contained in a table, **[The shared memory further includes a routing table, a configuration table, and a connection table, (Column 6, lines 55 – 56)].**

- Regarding claim 47, Lin teaches a device further comprising means adapted to insert a communication connection state into a packet to be routed, **[As also known in the art, a router is a device that routes data packets between networks. Routers read the network address in each transmitted data**

packet and make a decision on how to send it based on the most expedient route, (Column 4, lines 41 – 45)].

- Regarding claim 48, Lin teaches a device wherein the processing units are comprised of multi core digital signal processing means having shared data storage for all cores, **[Fig. 2 & 3].**

  whereby said device comprises a first level of load balancing for selecting a digital signal processing means and a second level of load balancing for selecting a single core, **[FIG. 10 is a block diagram illustrating a third embodiment of the invention having a user-level network interface for applications operating on the switching processor, (Column 3, lines 53 – 55)].**

- Regarding claim 49, Lin teaches a device further comprising means for redirecting excess traffic to another device, wherein said excess traffic is defined upon the number of active processing units, **[Routers read the network address in each transmitted data packet and make a decision on how to send it based on the most expedient route (traffic load, line costs, speed, bad lines, etc.), (Column 4, lines 43 – 46)].**

- Regarding claim 50, Lin teaches a system configured to obtain a current connection state as well as a current load state of said processing units from said

data storage, **[The switching processor obtains the current load distribution data from the active buffer, (Column 7, lines 12 – 13)]**;

selecting by said load balancing unit a processing unit on a per packet basis irrespective of a specific connection to which a respective packet belongs, **[In addition, the switching processors re-write the routing information included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract)]**;

maintaining information about the load state of each processing unit, **[A routing daemon within the control processor is a program that executes in the background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)]**;

so that said selecting step is performed by selecting a processing unit to serve and process a respective packet based on the load state, **[The switching processors route received ones of the data packets to a selected one of the external networks in accordance with information included in a header portion of the data packets and the load distribution configuration data, (See Abstract)]**.

- Regarding claim 51, Lin teaches a computer program embodied on a computer readable medium, the computer readable medium storing code comprising computer executable instructions configured to perform a method for balancing

the load of resources in a packet switched connection, **[A data packet switching and server load balancing device is provided by a general-purpose multiprocessor computer system, (See Abstract)];**

within a communication system **[respective external networks for receiving and sending data packets via a particular communication protocol, (See Abstract)];**

said system comprising processing units for performing communication, **[computer system comprises a plurality of symmetrical processors coupled together by a common data bus, (See Abstract)],** at least one load balancing unit for distributing the load to said processing units, **[The control processor receives raw load status data from the external networks and generates load distribution configuration data therefrom, (See Abstract)];**

and a data storage, **[a main memory shared by the processors, (See Abstract)];**

said method comprising: obtaining a current connection state as well as a current load state of said processing units from said data storage, **[The switching processor obtains the current load distribution data from the active buffer, (Column 7, lines 12 – 13)];**

selecting by said load balancing unit a processing unit on a per packet basis irrespective of a specific connection to which a respective packet belongs, **[In addition, the switching processors re-write the routing information**

included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract)];

maintaining information about the load state of each processing unit, **[A routing daemon within the control processor is a program that executes in the background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)];**

so that said selecting step is performed by selecting a processing unit to serve and process a respective packet based on the load state, **[The switching processors route received ones of the data packets to a selected one of the external networks in accordance with information included in a header portion of the data packets and the load distribution configuration data, (See Abstract)].**

- Regarding claim 52, Lin teaches a system comprising processing units performing communication, **[A data packet switching and server load balancing device is provided by a general-purpose multiprocessor computer system, (See Abstract)]**;

  and at least one load balancing unit for distributing the load to said processing units, **[Fig. 1, Ref # 10]**;

  a data storage, **[Fig. 4, Ref # 34]**;

  wherein the load-balancing unit is configured to: obtain a current connection state and a current load state of said processing units from said data storage, **[The switching processor obtains the current load distribution data from the active buffer, (Column 7, lines 12 – 13) & (Fig. 13, Ref # 342)]**;

  maintain information about the load state of each of said processing units, **[A routing daemon within the control processor is a program that executes in the background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)]**;

  and select a processing unit on a per packet basis irrespective of a specific connection to which a respective packet belongs by selecting one of the processing units to serve and process a respective packet based on the load state, **[In addition, the switching processors re-write the routing information**

included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract) & Fig. 3, Ref # 20 wherein a unit per packet is disclosed].

- Regarding claim 53, Lin teaches a load balancing unit is configured to:

  obtain a current connection state and a current load state of each of a plurality of processing units, **[The switching processor obtains the current load distribution data from the active buffer, (Column 7, lines 12 – 13) & (Fig. 13, Ref # 342)];**

  maintain information about the load state of each of said processing units, **[A routing daemon within the control processor is a program that executes in the background to retrieve the information stored in the routing table and maintains the status of the routing table as changes are made to the configuration, (Column 6, lines 63 – 67)];**

  and select a processing unit on a per packet basis irrespective of a specific connection to which a respective packet belongs by selecting one of the processing units to serve and process a respective packet based on the load state of the selected processing unit, **[In addition, the switching processors re-write the routing information included in the header portion of the data packets to reflect the selected one of the external networks, (See Abstract) & Fig. 3, Ref # 20 wherein a unit per packet is disclosed].**

Conclusion

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **PEP 707.05(c)**.

The following are analogous art because they are from the same field of endeavor of Load Balancing Device and Method Therefor:

- Lin et al. Paten No: (US 6,272,522)
- Bowman-Amuah et al. Patent No: (US 6,578,068)
- Budka et al. Paten No: (US 6,014,567)
- Eriksson et al. Paten No: (US 6,385,449)
- Kotzin et al. Patent No: (US 5,796,722)
- Broder et al. Patent No: (5,991,808)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Shaq Taha** whose telephone number is 571-270-1921. The examiner can normally be reached on 8:30am-5pm Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jeff Put** can be reached on 571-272-6798.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/08/07

S. Taha

JEFFREY PWU
SUPERVISORY PATENT EXAMINER